IN THE CLAIMS

Please amend the claims as follows:

Claims 1 (Canceled).

Claim 2 (Currently Amended): The information storage device according to claim [[1]] 3, wherein the frequency of said synchronizing clock signal is variable.

Claim 3 (Currently Amended): ~~The information storage device according to claim 1,~~ An information storage device comprising:

a plurality of memory cells configured to store data by accumulating an electrical charge; and

an amplifier configured to amplify the electrical charge of the memory cells,

wherein a synchronizing clock signal is used for input/output timing of the data; and

wherein an electrical charge removal operation for moving the electrical charge of said memory cells to said amplifier or an electrical charge accumulation operation for acquiring the electrical charge from said amplifier and accumulating the electrical charge of said memory cells and an input/output operation for said amplifier in relation to the outside of the information storage device are processed while using a single clock of said synchronizing clock signal for synchronization timing,

wherein said operations begin when a request signal is received; and wherein, when said request signal is received, the address of a memory cell related to the request signal is compared against the address of data temporarily retained in said amplifier at the time of request signal reception.

Claim 4 (Currently Amended): An information storage device comprising:

a plurality of memory cells ~~for storing~~ configured to store data by accumulating an electrical charge;

an amplifier ~~for amplifying~~ configured to amplify the electrical charge of the memory cells; and

a comparator ~~for comparing~~ configured to compare a requested memory cell address against data temporarily retained in said amplifier,

wherein, if the requested memory cell address does not agree with the address of the data in said amplifier, instructions are issued for sequentially processing an electrical charge accumulation operation for acquiring [[an]] the electrical charge from said amplifier and accumulating the electrical charge [[in]] of said memory cells, an input/output operation for said amplifier in relation to the outside of the information storage device, and an electrical charge removal operation for moving [[an]] the electrical charge [[from]] of said memory cells to said amplifier in order named while using a single clock for synchronization timing.

Claim 5 (Currently Amended): The information storage device according to claim 4, wherein, when nothing is retained by said amplifier, said comparator issues instructions for sequentially processing [[an]] the electrical charge removal operation for moving [[an]] the electrical charge from said memory cells to said amplifier and [[an]] the input/output operation for said amplifier in relation to the outside of the information storage device in order named while using a single clock for synchronization timing.

Claim 6 (Currently Amended): The information storage device according to claim 4, wherein, when the requested memory cell address agrees with the address of the data in said amplifier, said comparator issues instructions for processing [[an]] the input/output operation

for said amplifier in relation to the outside of the information storage device with clock synchronization achieved.

Claim 7 (Original): The information storage device according to claim 4, wherein the frequency of said synchronizing clock signal is variable.

Claim 8 (Currently Amended): An information storage device comprising:

a plurality of memory cells ~~for storing~~ configured to store data by accumulating an electrical charge;

an amplifier ~~for amplifying~~ configured to amplify the electrical charge of the memory cells; and

a comparator ~~for comparing~~ configured to compare a requested memory cell address against data in said amplifier, and ~~performs~~ configured to perform, on every single clock of a synchronizing clock signal, an electrical charge removal operation for moving [[an]] the electrical charge [[from]] of said memory cells to said amplifier, an electrical charge accumulation operation for acquiring [[an]] the electrical charge from said amplifier and accumulating the electrical charge [[in]] of the memory cells, and an input/output operation for said amplifier in relation to the outside of the information storage device.

wherein, if the requested memory cell address ~~agrees~~ does not agree with the address of the data in said amplifier, instructions are issued for sequentially processing [[an]] the electrical charge accumulation operation for acquiring [[an]] the electrical charge from said amplifier and accumulating the electrical charge [[in]] of said memory cells, [[an]] the input/output operation for said amplifier in relation to the outside of the information storage device, and [[an]] the electrical charge removal operation for moving [[an]] the electrical

charge [[from]] of said memory cells to said amplifier in order named while using a single clock of said synchronizing clock signal for synchronization timing.

Claim 9 (Original): The information storage device according to claim 8, wherein the frequency of said synchronizing clock signal is variable.

Claim 10 (Currently Amended): The information storage device according to claim 8, wherein, in accordance with the frequency of said synchronizing clock signal, said comparator issues instructions for sequentially processing [[an]] the electrical charge accumulation operation for acquiring [[an]] the electrical charge from said amplifier and accumulating the electrical charge in said memory cells and [[an]] the input/output operation for said amplifier in relation to the outside of the information storage device in order named, and for sequentially processing [[an]] the input/output operation for said amplifier in relation to the outside of the information storage device and [[an]] the electrical charge accumulation operation for acquiring [[an]] the electrical charge from said amplifier and accumulating the electrical charge in said memory cells in order named.

Claim 11 (Currently Amended): An information storage method comprising ~~the steps of~~:

comparing, when a request signal is received, the memory cell address designated by the request signal against the address of data temporarily retained in an amplifier; and

selectively performing, in accordance with the comparison result, an electrical charge removal operation for moving an electrical charge from said memory cells to said amplifier, an electrical charge accumulation operation for acquiring an electrical charge from said

amplifier and accumulating the electrical charge in said memory cells, and an input/output operation for said amplifier in relation to the outside of the information storage device.

Claim 12 (Currently Amended): The information storage method according to claim 11, wherein ~~the step of~~ said selectively performing said operations is processed while using substantially the same clock of a synchronizing clock signal for synchronization timing.

Claim 13 (Original): The information storage method according to claim 11, wherein the frequency of said synchronizing clock signal is variable.

Claim 14 (Original): The information storage method according to claim 11, wherein said selectively performed operations comprise a process that is a combination of two or more operations.

Claim 15 (Currently Amended): An information storage program for executing an information storage method ~~that comprises the steps of~~ comprising:

comparing, when a request signal is received, the memory cell address designated by the request signal against the address of data temporarily retained in an amplifier; and

selectively performing, in accordance with the comparison result, an electrical charge removal operation for moving an electrical charge from said memory cells to said amplifier, an electrical charge accumulation operation for acquiring an electrical charge from said amplifier and accumulating the electrical charge in said memory cells, and an input/output operation for said amplifier in relation to the outside of the information storage device.

Claim 16 (Currently Amended): The information storage program according to claim 15, wherein ~~the step of~~ said selectively performing said operations is processed while using substantially the same clock of a synchronizing clock signal for synchronization timing.

Claim 17 (Original): The information storage program according to claim 15, wherein said selectively performed operations comprise a process that is a combination of two or more operations.